Claims

[1] A semiconductor device comprising:
a first active region comprising a plurality of slabs formed on a substrate, each slab having a first surface, a second surface facing a direction opposite to the first surface, and a top surface;
a second active region contacting at least one end of each of the slabs on the substrate to connect the slabs to one another;
a gate line formed on the first surface, the second surface and the top surface of each of the slabs; and
a gate dielectric layer interposed between the slabs and the gate line.
The semiconductor device of claim 1, wherein the first active region is formed in a line-and-space pattern.

[2] The semiconductor device of claim 1, wherein the first active region is formed in a line-and-space pattern.

[3] The semiconductor device of claim 1, wherein the first active region and the second active region are composed of different materials.

[4] The semiconductor device of claim 1, wherein the top surface of each of the slabs is disposed a first distance above the substrate, and a top surface of the second active region is disposed a second distance above the substrate, the second distance being equal to or greater than the first distance

[5] The semiconductor device of claim 4, wherein the second distance is greater than the first distance.

[6] The semiconductor device of claim 4, wherein the second distance is equal to the first distance.

[7] The semiconductor device of claim 1, wherein the second active region contacts both ends of each of the slabs and extends in a direction orthogonal to a direction in which the slabs extend.

[8] The semiconductor device of claim 1, wherein the second active region has an overlap region that contacts a portion of the first surface, the second surface and the top surface of each of the slabs.

[9] The semiconductor device of claim 1, wherein the first active region is composed of monocrystalline silicon, and the second active region is composed of polysilicon, amorphous silicon, or a semiconductor compound containing silicon.

[10] The semiconductor device of claim 1, wherein the first active region and the second active region form a source/drain region.

[11] The semiconductor device of claim 1, wherein the first active region

comprises a channel region.

[12] The semiconductor device of claim 1, wherein the gate line extends in a direction orthogonal to the direction in which the slabs extend.

[13] The semiconductor device of claim 1, wherein the gate line extends parallel to the direction in which the second active region extends.

[14] The semiconductor device of claim 1, wherein the gate line is composed of conductive polysilicon, metal, metallic nitride, or metal silicide.

[15] The semiconductor device of claim 1, wherein the gate dielectric layer contains SiO_2, SiON, Si_3N_4, $Ge_xO_yN_z$, $Ge_xSi_yO_z$, HfO_2, ZrO_2, Al_2O_3, TiO_2, or Ta_2O_5.

[16] The semiconductor device of claim 1, wherein the substrate is a silicon-on-insulator substrate comprising a buried oxide layer and a silicon layer, and the first active region and the second active region are formed on the buried oxide layer.

[17] The semiconductor device of claim 1, further comprising a first channel region and a second channel region respectively adjacent to the first surface and the second surface of each of the slabs in the first active region and facing the gate line.

[18] The semiconductor device of claim 17, further comprising a third channel region adjacent to the top surface of each of the slabs in the first active region and facing the gate line.

[19] A method of manufacturing a semiconductor, the method comprising:
forming a first active region on a substrate, the first active region being composed of a first material;
forming a second active region on the substrate, the second active region contacting at least a portion of the first active region and being composed of a second material;
forming a gate dielectric layer on the first active region; and
forming a gate on the gate dielectric layer.

[20] The method of claim 19, wherein the first active region is formed in a line-and-space pattern.

[21] The method of claim 19, wherein the first material and the second material are different from each other.

[22] The method of claim 19, wherein the forming the first active region comprises forming a plurality of slabs extending on the substrate in a first direction, each slab having a first surface, a second surface facing a direction opposite to the first side, and a top surface.

[23] The method of claim 22, wherein the top surface of each of the

slabs is disposed a first distance above the substrate, and a top surface of the second active region is disposed a second distance above the substrate, the second distance being equal to or greater than the first distance.

[24] The method of claim 22, wherein the second active region contacts both ends of the slabs and extends in a second direction orthogonal to the first direction.

[25] The method of claim 22, wherein the second active region has an overlap region that contacts a portion of the first surface, the second surface and the top surface of each of the slabs.

[26] The method of claim 22, wherein the forming the second active region comprises:
forming a mask pattern covering a portion of each of the slabs on the substrate such that both of the ends of each of the slabs are exposed;
forming a second material layer covering both of the exposed ends of each of the slabs and the mask pattern by depositing the second material; and
forming the second active region by planarizing the second material layer.

[27] The method of claim 26, wherein the mask pattern is an SiON layer, an Si_3N_4 layer, or an SiO_2 layer, or a combination of the same.

[28] The method of claim 27, wherein the mask pattern includes an SiON layer and an Si_3N_4 layer stacked sequentially.

[29] The method of claim 26, wherein the mask pattern covers only a portion of the top surface of each of the slabs such that the top surface of each of the slabs can be partially exposed around the mask pattern after the mask pattern is formed.

[30] The method of claim 26, wherein the second material layer is planarized using the mask pattern as an etch-stop layer.

[31] The method of claim 30, wherein the mask pattern comprises an SiON layer contacting each of the slabs and an Si_3N_4 layer forming a top surface of the mask pattern.

[32] The method of claim 26, wherein the second material layer is planarized by chemical mechanical polishing or back etching.

[33] The method of claim 19, wherein the first material is monocrystalline silicon, and the second material is polysilicon, amorphous silicon, or a semi-conductor compound containing silicon.

[34] The method of claim 19, wherein the gate dielectric layer contains SiO_2, SiON, Si_3N_4, $Ge_xO_yN_z$, $Ge_xSi_yO_z$, HfO_2, ZrO_2, Al_2O_3, TiO_2, or Ta_2O_5.

[35] The method of claim 22, wherein the forming the gate includes forming a gate line extending in a second direction orthogonal to the first direction such

that the gate line covers the fist surface, the second surface and the top surface of each of the slabs to form the gate.

[36] The method of claim 35, wherein the gate line is composed of conductive polysilicon, metal, metallic nitride, or metal silicide.

[37] The method of claim 19, further comprising preparing a silicon-on-insulator substrate as the substrate, the silicon-on-insulator substrate comprising a buried oxide layer and a monocrystalline silicon layer formed on the buried oxide layer, and the first active region is formed by patterning the monocrystalline silicon layer.